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10/573,970	03/30/2006	Tatsuo Hiramatsu	070456-0105	1749

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EXAMINER	
GIROUX, GEORGE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,970	HIRAMATSU ET AL.	
	Examiner	Art Unit	
	GEORGE D. GIROUX	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34 and 37-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34 and 37-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed 26 February 2009, in response to the Office Action mailed 26 November 2008. The applicant's remarks and amendments to the claims and specification were considered, with the results that follow.

2. Claims 1-33, 35 and 36 have been cancelled, while new claims 44-48 have been added. Claims 34 and 37-48 are now pending in this application.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 26 February 2009 has been entered.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claim 34 is objected to because of the following informalities: on page 3, line 7, the "(i+1) state holding circuit" appears as if it should read "(i+1)th state holding circuit" with the rest of the claim. Appropriate correction is required.

6. Claim 48 is objected to because of the following informalities: "t.o claim 44" on the first line should read "to claim 44". Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 34 and 37-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Abramovici (US 6,034,538).

As per claim 34, Abramovici teaches a reconfigurable circuit allowing change in function and connection relation as **[a set of reconfigurable hardware including a number of field programmable gate arrays (FPGAs) (figure 2 and abstract)]**, a setting portion storing setting data representing a divided unit forming a part of a circuit and supplying the setting data to the reconfigurable circuit as **[the local memory includes dedicated areas for storing configuration information (column 4, lines 13-15 and figure 2) which is supplied, via the page manager, to the FPGAs**

(column 5, lines 3-5 and figure 2)], a control portion controlling the setting portion such that a plurality of setting data are successively supplied to the reconfigurable circuit to configure the intended circuit as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10)]**, wherein the reconfigurable circuit has N state holding circuits holding an internal state as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages, where the PAGMAN 22 may include one or more FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50)]**, said reconfigurable circuit is divided by an arrangement of said N state holding circuits into N+1 stages of reconfigurable units as **[each page (which may be loaded onto the FPGA) is a subcircuit of the logic circuit created by partitioning the initial netlist, which may correspond to stages of an overall circuit, but does not necessarily require any particular functional relationship between pages (column 3, lines 32-55) where the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and**

is operative to route signals between loaded pages, where the PAGMAN 22 may include one or more FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50)], said control portion controls said setting portion such that, when a plurality of intended circuits are to be configured, setting data for configuring divided units each forming a part of the circuits on respective ones of said plurality of stages of reconfigurable units are successively supplied along a process flow as **[each page (which may be loaded onto the FPGA) is a subcircuit of the logic circuit created by partitioning the initial netlist, which may correspond to stages of an overall circuit, but does not necessarily require any particular functional relationship between pages (column 3, lines 32-55)]**, and the control portion controls said setting portion such that at one time point, setting data of a divided circuit unit configuring an intended circuit is supplied to a reconfigurable unit between the i-th state holding circuit and the (i+1)th state holding circuit as **[a given subcircuit is implemented in a part of the reconfigurable hardware by loading its corresponding page into the hardware, referred to as a loaded page, where the page manager is used to control the loading of the page to and from the reconfigurable hardware (column 3, lines 56-67) where the PAGMAN 22 may include one or more FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50)]**, said control portion controls said setting portion such that at a next time point, setting data of a next divided unit configuring said intended circuit is supplied to said reconfigurable unit between the (i+1)th state holding circuit and the (i+2)th state holding

circuit in accordance with the process flow as **[a page configuration for a circuit which includes a feed-forward structure, where the outputs of one page loaded into the FPGAs feed the input of the next page loaded into the FPGAs (column 6, lines 31-44 and figure 5A) where the PAGMAN 22 may include one or more FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50)]**, said control portion controls said setting portion such that at said next time point, setting data of a divided unit configuring a different intended circuit is supplied to said reconfigurable unit between the i-th state holding circuit and the (i+1)th state holding circuit as **[a page replacement algorithm may be used to select a replacement page for a currently loaded page, where the PAGMAN saves all of the register values of the page to be replaced and disconnects all of the I/O pins associated with that page, then the configuration of the new, replacing page is sent to the reconfigurable hardware, by the PAGMAN, from the local memory (column 5, line 59 through column 6, line 9)]**.

As per claim 37, Abramovici teaches wherein the reconfigurable unit is configured as a combinational circuit as **[the reconfigurable hardware can be made of a number of any commercially available FPGAs or via a single FPGA (column 4, lines 39-52) which are inherently formed of logic blocks operating via combinational functions, forming a combinational circuit]**.

As per claim 38, Abramovici teaches an output circuit receiving an output of the reconfigurable circuit as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)]** and providing the output of the reconfigurable circuit when the reconfigurable circuit is configured a plurality of times by the setting portion as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAS and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)]**.

As per claim 39, Abramovici teaches an internal state holding circuit receiving an output of the reconfigurable circuit and a first path portion inputting the output signal held by said internal state holding circuit to the first stage of reconfigurable units as **[the page manager (PAGMAN 22) includes one or more first-in-first-out (FIFO) buffers for use in controlling storage and transferring inter-page signal values (i.e. storing the output of one page, to be provided as the input to another) (column 5, lines 10-21 and figure 3)]**.

As per claim 40, Abramovici teaches a memory portion storing in a prescribed area an output of said reconfigurable circuit in accordance with setting data as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the**

page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)] and a second path portion transmitting the output of the circuit configured on the reconfigurable circuit, which is stored in the memory portion, as an input to a circuit configured in accordance with the next setting data as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)]**.

As per claim 41, Abramovici teaches a switching circuit switching between the input from said second path portion and an external input, to be an input to said reconfigurable circuit as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2) where the page manager directs the connecting and disconnecting of the I/O pins of the FPGA being configured (column 5, lines 63-65) including the connections to various other types of external non-FPGA hardware (column 4, lines 51-56) which inherently includes inputs available from the connected hardware]**.

As per claim 42, Abramovici teaches wherein the reconfigurable unit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions as **[the reconfigurable hardware 20 is composed of a number of FPGAs (column 4, lines 3-9 and figure 2) where FPGAs are inherently capable of execution a plurality of functions]**, a connection portion allowing setting of connection relations among the logic circuits as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) as well as controlling storage and transfer of information between the FPGAs (abstract)]** and said setting portion sets the functions and said connection relation of said logic circuits as **[the page manager controls loading and unloading of pages form the local memory into the FPGAs and controls storage and transfer between the FPGAs (abstract)]**.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici (US 6,034,538) in view of Mansingh (US 6745318).

As per claim 43, Abramovici teaches the processing device according to claims 42, as described above.

Abramovici does not explicitly teach wherein the logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations, however.

Mansingh teaches wherein the logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations as **[a dynamic arithmetic unit 18, including at least one configurable arithmetic unit 20 capable of performing operations from decoded instructions 24, provided by the decoder 16 (column 2, lines 38-47 and figure 1)]**.

Abramovici and Mansingh are analogous art, as they are within the same field of endeavor, namely reconfigurable processing.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use the configurable arithmetic logic unit of Mansingh in the reconfigurable circuit of Abramovici.

The motivation for doing so, as provided by Mansingh, would have been **[to decrease the size of the combined arithmetic logic units' integrated circuit footprint by providing a single reconfigurable arithmetic logic unit, thus reducing costs (column 1, lines 48-54)]**.

11. Claims 44-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici (US 6,034,538) in view of well known practices in the art.

As per claim 44, Abramovici teaches a reconfigurable circuit capable of arranging a circuit that can be divided into at least three divided circuits successively on a same region in an order of a first divided circuit, a second divided circuit and a third divided circuit as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) where the logic circuit netlist is partitioned into a number of disjoint subcircuits, with each of the subcircuits represented by a portion of the initial netlist generally referred to herein as a "page" and the partitioning of the logic circuit into subcircuits is thus implemented by partitioning the initial netlist into corresponding pages (column 3, lines 32-55) where each of the stages of the logic circuit can be applied, in turn to the same reconfigurable hardware (column 1, lines 42-64)]**, a memory portion storing an output of said reconfigurable circuit as **[the FPGAs and the page manager communicate via bus 23 with the local memory 24 which holds output and register values from the FPGAs, as well as the configuration information (column 4, lines 8-19 and figure 2)]**, a state holding portion, and storing an output of said reconfigurable circuit as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages, where the PAGMAN 22 may include one or more**

FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50)], and a switching portion selecting an output of said memory portion and an output of said state holding portion, and supplying the selected output to said reconfigurable circuit as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2) where the page manager directs the connecting and disconnecting of the I/O pins of the FPGA being configured (column 5, lines 63-65)]**, wherein said third divided circuit can be further divided into a fourth divided circuit and a fifth divided circuit and allows arrangement successively on a same region in an order of said forth divided circuit and said fifth divided circuit as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) where the logic circuit netlist is partitioned into a number of disjoint subcircuits, with each of the subcircuits represented by a portion of the initial netlist generally referred to herein as a "page" and the partitioning of the logic circuit into subcircuits is thus implemented by partitioning the initial netlist into corresponding pages (column 3, lines 32-55) where each of the stages of the logic circuit can be applied, in turn to the same reconfigurable hardware (column 1, lines 42-64)]**, when said fourth

divided circuit is arranged on said reconfigurable circuit, said switching portion supplies an output of said first and second divided circuits stored in said memory portion to said reconfigurable circuit as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages, where the PAGMAN 22 may include one or more FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50)]**, and when said fifth divided circuit is arranged on said reconfigurable circuit, an output of said fourth divided circuit held in said state holding portion is supplied to said reconfigurable circuit as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages, where the PAGMAN 22 may include one or more FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50)]**.

Abramovici does not explicitly teach wherein the state holding portion operates faster than said memory portion, but does teach **[that the type of memory used for local memory 24 may limit the speed of the system and slow down processing (column 4, lines 57-67)]**.

However, the examiner takes official notice that it would have been obvious to one of ordinary skill in the art, at the time the invention was made, that the memory portion operates at a lower speed than the internal state holding portion, as it is well known in the art that the larger the memory and the further from the processor, the longer the access time, and likely the slower the memory.

As per claim 45, Abramovici teaches wherein said reconfigurable circuit is configured as a combination circuit as **[the reconfigurable hardware can be made of a number of any commercially available FPGAs or via a single FPGA (column 4, lines 39-52) which are inherently formed of logic blocks operating via combinational functions, forming a combinational circuit]**.

As per claim 46, Abramovici teaches wherein said reconfigurable circuit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions as **[the reconfigurable hardware 20 is composed of a number of FPGAs (column 4, lines 3-9 and figure 2) where FPGAs are inherently capable of execution a plurality of functions]** and a connecting portion allowing setting of connection relation among the logic circuits as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route**

signals between loaded pages (column 5, lines 3-10) as well as controlling storage and transfer of information between the FPGAs (abstract)].

12. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici (US 6,034,538) in view of well known practices in the art, and further in view of Mansingh (US 6745318).

As per claim 47, Abramovici teaches the processing device according to claim 46, as described above.

Abramovici does not explicitly teach wherein the logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations, however.

Mansingh teaches wherein the logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations as **[a dynamic arithmetic unit 18, including at least one configurable arithmetic unit 20 capable of performing operations from decoded instructions 24, provided by the decoder 16 (column 2, lines 38-47 and figure 1)]**.

Abramovici and Mansingh are analogous art, as they are within the same field of endeavor, namely reconfigurable processing.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use the configurable arithmetic logic unit of Mansingh in the reconfigurable circuit of Abramovici.

The motivation for doing so, as provided by Mansingh, would have been **[to decrease the size of the combined arithmetic logic units' integrated circuit**

footprint by providing a single reconfigurable arithmetic logic unit, thus reducing costs (column 1, lines 48-54)].

13. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici (US 6,034,538) in view of well known practices in the art, and further in view of Kim (US 2005/0135508).

As per claim 48, Abramovici teaches the processing device according to claim 44, as described above.

Abramovici does not explicitly teach wherein said processing device is a digital demodulating device, said first dividing circuit is a filter circuit processing an I signal, said second divided circuit is a filter circuit processing a Q signal, and said third divided circuit is a demodulating circuit including a loop filter, a multiplier and a positive/negative determining circuit.

Kim teaches wherein said processing device is a digital demodulating device as **[carrier recovery apparatus, including demodulator (figure 11)]**, said first dividing circuit is a filter circuit processing an I signal and as **[a first low pass filter 603a for passing a pilot component of I signal included in the I baseband signal from the complex multiplier 602 (figure 11 and paragraph 0132)]**, said second divided circuit is a filter circuit processing a Q signal as **[a second low pass filter 603b for eliminating a data component in the Q baseband signal from the complex multiplier 602 (figure 11 and paragraph 0132)]**, and said third divided circuit is a demodulating circuit including a loop filter, a multiplier and a positive/negative

determining circuit as **[carrier recovery apparatus, including demodulator, loop filter and sign extractor (for positive/negative determining) (figure 11)]**.

Abramovici and Kim are analogous art, as they are within the same field of endeavor, namely signal processing.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to configure the reconfigurable processors of Abramovici to process the carrier signal demodulation operations taught by Kim.

All of the component parts are taught by Abramovici and Kim, the only difference is using the general processor of Abramovici to achieve the specific type of processing performed by Kim. Thus, it would have been obvious to one of ordinary skill in the art to configure the reconfigurable processors of Abramovici to process the carrier signal demodulation operations taught by Kim, to achieve the predictable result of performing the demodulation processing on carrier signals. Kim further teaches that **[the components can eliminate unnecessary sign extraction caused by zero-crossing which is generated when the receiver receives a pilot signal weaken by a channel ghost, and improves the frequency lock performance in a receiver (abstract)]**.

Response to Arguments

14. Applicant's arguments filed 26 February 2009 have been fully considered but they are not persuasive.

15. Applicant argues that Abramovici does not carry out a plurality of processes in parallel.

However, Abramovici teaches each page (which may be loaded onto the FPGA) is a subcircuit of the logic circuit created by partitioning the initial netlist, which may correspond to stages of an overall circuit, but does not necessarily require any particular functional relationship between pages (column 3, lines 32-55) where the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages, where the PAGMAN 22 may include one or more FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50), where each FPGA may be loaded and processing from a page, and the FIFO buffers at the input of the other FPGAs will be filling, in parallel, with the output data (column 5, lines 23-50).

Conclusion

16. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**: claims 1-33, 35 and 36 have been cancelled; claims 34 and 37-48 are rejected.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Serrano (US 2006/0126454) -- discloses processing for a demodulator, including a loop filter and positive/negative peak determination.

b. Naoi (US 2003/0200237) -- discloses a pipeline of programmable arithmetic logic units that can be controlled individually or operated together and work in a cascade fashion.

c. Vorbach (US 2006/0248317) - teaches a reconfigurable circuit which can be divided dynamically to perform given operations.

d. Vorbach (US 7,003,660) -- discloses pipelining configurable processing units.

e. Pickett (US 4,942,319) -- discloses multiple programmable pages configured into a programmable array, including moving signals between.

18. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

19. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GEORGE D. GIROUX whose telephone number is (571)272-9769. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/George D Giroux/
Examiner, Art Unit 2183